AN-728
Application Note

13-WATT MICROSTRIP AMPLIFIER FOR 220–225 MHz OPERATION

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Design, performance and construction information are provided for a 12.5 volt, FM Transmitter power amplifier and low pass filter. MRF225 and MRF226 RF power transistors are utilized in the two-stage amplifier to achieve 13 watts of power output to the filter from approximately 125 mW of drive at 225 MHz. Economical dipped-mica capacitors, microstrip lines and eyelet construction have been employed.

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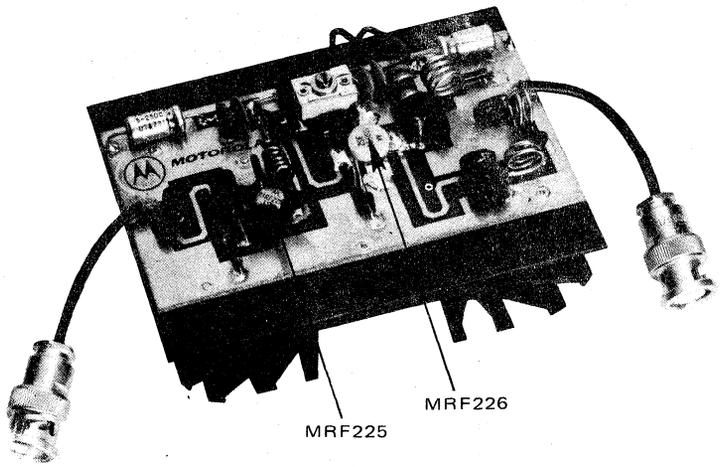


COMPLETED AMPLIFIER

13-WATT MICROSTRIP AMPLIFIER FOR 220–225 MHz OPERATION

INTRODUCTION

This report describes performance and design techniques for a 225 MHz, 12.5 V, FM Transmitter power amplifier and low pass filter. 13 W of power output to the filter assures ample reserve for supplying a consistent 10 W of power to the transmitting antenna. Since the ±0.5 dB bandwidth is approximately 10 MHz, the design is well suited for use in transmitters for the 220-225 MHz Amateur Radio Band or the proposed "Class E" Citizens Band.

HIGHLIGHTS

- Low pass filter provides approximately 60 dB total attenuation to 2nd Harmonic.
- Economical components such as dipped-silvered mica capacitors used throughout.
- Microstrip matching network design enhances reproducibility and minimizes cost.
- Evaluation data for open/short circuit load conditions at all phase angles and high line voltage (15.5 Vdc) is included.
- Printed circuit board layout suitable for economical eyelet and wave-soldering assembly techniques is provided.

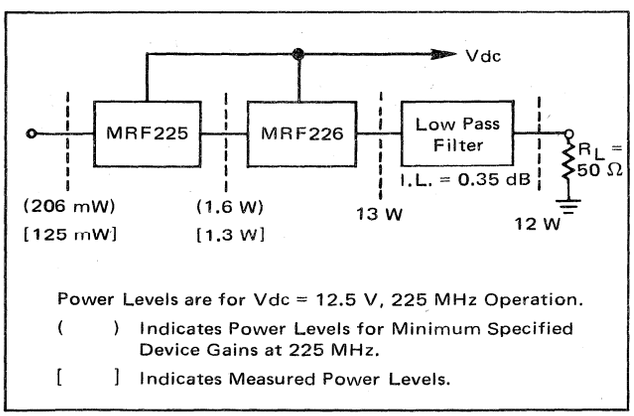


FIGURE 1 – Amplifier Block Diagram Showing Stage-by-Stage Power Levels

DEVICE CONSIDERATIONS

The MRF225 and MRF226 RF power transistors have been specially processed and characterized by Motorola for use in the frequency range of interest. They are rated for 1.5 and 13 W of power output respectively and minimum power gains of 9.0 dB at 225 MHz. The standard package for the MRF226 is the 0.380-inch diameter, stripline-opposed-emitter (SOE), case 145A-01. A TO-39 package is used for the MRF225.

Large signal series impedance parameters for the transistors, as provided by the device data sheets, are given in Table I. For a complete discussion regarding the use of large signal characterization, See Reference 1.

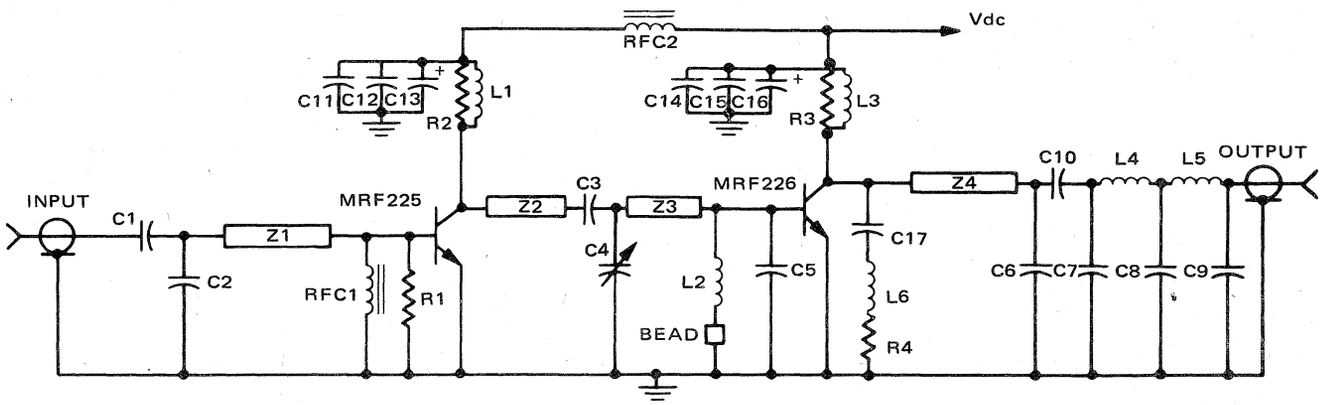
Approximate power levels when the amplifier is supplying 13 W to the low pass filter input are given on the block diagram in Figure 1. Both expected worst case power levels, as determined from the minimum specified device gains, and the typical power levels actually measured for constructed amplifiers have been included.

CIRCUIT DESCRIPTION

Figure 2 is a complete schematic for the amplifier, together with a list of components and the overall test results. Both transistor stages are of the grounded-emitter configuration and are operated class C. Circuit component

TABLE I – LARGE SIGNAL SERIES IMPEDANCE DATA FOR RATED P_{out} AT 225 MHz AND Vdc = 12.5 V

DEVICE	INPUT IMPEDANCE Z_{in} (Ω)	OUTPUT IMPEDANCE Z_{out} (Ω)
MRF225	5.8 – j 5.2	22 – j 33.5
MRF226	1.7 + j 0.2	6.6 – j 3.7



Components List

C1 – 10 pF
C2, C3 – 15 pF
C5 – 68 pF
C6 – 18 pF
C7, C9 – 12 pF
C8, C10 – 20 pF
C17 – 82 pF
} Dipped Silvered Mica, El-Menco Case DM10

C11, 14 – .01 μF Ceramic Disc
C12, 15 – 220 pF Ceramic Disc
C13, 16 – 5 μF, 25 V, Aluminum Electrolytic
C4 – 3-35 pF Trimmer, ARCO NO. 403
L1 – 5 T NO. 20 AWG Wire, Wound on R2 (50 nH)
L2 – 1.5 T NO. 20 AWG Wire, 0.25-In. I.D. (30 nH) with Ferroxcube 5659065/3B Ferrite Bead
L3 – 2 T NO. 20 AWG Wire, Wound on R3 (35 nH)
L4, 5 – 2 T NO. 18 AWG Wire, 0.25-In. I.D. (44 nH)
L6 – 3.5 T NO. 18 AWG Wire, 0.25-In. I.D. (90 nH)
R1 – 100 Ohm, 1/4 W, ±10% Carbon Resistor
R2 – 820 Ohm, 1/2 W, ±10% Carbon Resistor
R3 – 330 Ohm, 1 W, ±10% Carbon Resistor
R4 – 22 Ohm, 1/4 W, ±10% Carbon Resistor
RFC1, 2 – Ferroxcube VK200 19/4B Choke

Z1 – Microstrip Line, 2200 X 62 Mils
Z2 – Microstrip Line, 1200 X 62 Mils
Z3 – Microstrip Line, 1000 X 62 Mils
Z4 – Microstrip Line, 1600 X 62 Mils
Board – G10 Epoxy-Glass, ϵ_r = 5, t = 62 Mils 1 oz. Copper

Amplifier/Filter Test Data for f = 225 MHz, Vdc = 12.5 Volts
P_{out} = 12 W at Filter Output

P_{in} for P_{out} = 12 W at Filter Output	125 mW
Power Gain	19.6 dB
L. P. Filter insertion loss	0.35 dB
2nd Harmonic attenuation	60 dB
Bandwidth	4 MHz (for ±0.1 dB)
	10 MHz (for ±0.5 dB)
Efficiency	58 percent
Input VSWR	1.5:1
DC Current:	
Total	1.66 A
Output Stage	1.50 A
Input Stage	0.16 A

Stability: Stable for input drive levels from zero to more than 30% overdrive for Vdc values from 8.0 to 15.5 V.

Ruggedness: No transistor damage for open and short circuit load conditions for all load phases angles and high line of 15.5 V. Total amplifier current peaks and nulls at approximately 2.3 and 0.5 A respectively as the load phase angle is cycled.

FIGURE 2 – 225 MHz Amplifier/Filter Schematic Diagram, Components List and Test Results

values have been optimized to assure stable operation for wide variations of input power, dc supply voltage and load VSWR. A 45 MHz series trap consisting of C17, L6 and R4 eliminates any 40 to 50 MHz oscillations that may otherwise occur during open/short circuit load conditions for certain load-phase angles.

Allowance for unit-to-unit variations is made by including an adjustable component (C4) to optimize interstage matching, and resistor R1 to minimize input impedance variations. If desired, additional optimization of input VSWR can be achieved by using an adjustable capacitor for C2.

The five-element low pass filter consisting of C7, C8, C9, L4 and L5 provides approximately 30 dB additional attenuation to the second harmonic (450 MHz).

The component values specified for the dipped mica capacitors (EL-Menco, DM10) represent nominal low-frequency values. The effective capacitance of these components can be significantly different and will vary with lead length at VHF frequencies. The capacitors must therefore be characterized at the frequency of interest before a meaningful design procedure can take place. Table II provides representative capacitor data for 225 MHz operation.

TABLE II – CAPACITOR VALUES AT 225 MHz

NOMINAL LOW FREQUENCY CAPACITANCE (pF)	CAPACITANCE AT 225 MHz (pF)	PARALLEL REACTANCE COMPONENT AT 225 MHz (Ω)
10	12.5	56.6
12	15	47.2
15	19	37.2
20	26	27.2
24	30	23.6
68	145	4.9
3-35 (Variable)	5 – 130	141 – 5.4

Capacitor Type: Fixed – Dipped silvered mica, El Menco Type DM10 with each lead 1/16" in length.
Variable – ARCO #403 Compression Mica.

PERFORMANCE

The curves in Figure 3 provide evaluation information for the amplifier/filter combination. Figures 3A and 3B indicate power output and amplifier dc current as a function of input power for supply voltages of 12.5 V and 13.6 V respectively. Figure 3C shows power at filter output and amplifier dc current as a function of variable dc supply voltage.

High load VSWR testing has been performed at high line voltage without damage to either transistor. Figure 3D indicates the current and approximate power dissipation levels for the MRF226 output device when the filter output is mismatched into open and short circuit loads. This data was obtained by adjusting input power for 12 W output into a 50 Ω load at the filter output with Vdc=12.5 V. The dc supply was then increased to 15.5 V (resulting in 14.8 W of power output) and the 50 Ω load replaced with an open or short circuited air line of variable length. The length of the air line was then changed to subject the amplifier to all possible load-phase angles. The horizontal scale of the graph represents this change in line length. As indicated by the curves, worst case power dissipation for the MRF226 transistor is approximately 33 W. This is a significant increase from the normal 12.5 V, 50 Ω load value of about 7 W (Thermal Design Section – Equation 4). The transistor has been specially designed and manufactured to resist failure under these conditions. Prolonged operation in the worst case condition will, however, require a heat sink having a thermal

Evaluation Information for the Amplifier/Filter Combination

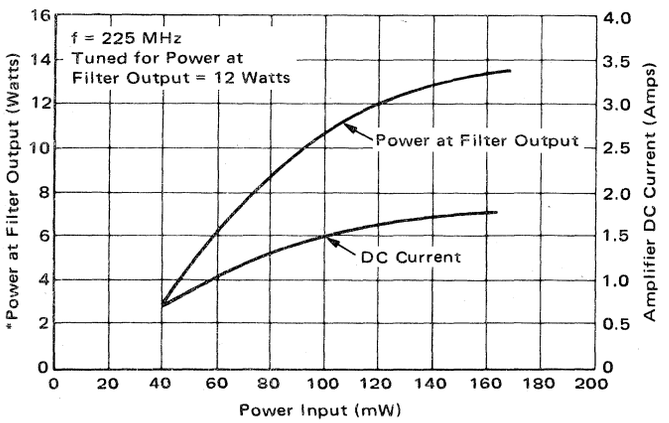


FIGURE 3A – Power at Filter Output and Amplifier dc Current Versus Power Input for Vdc = 12.5 V.

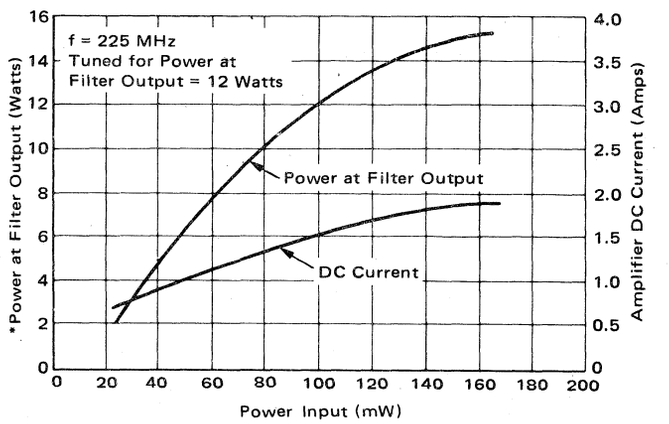


FIGURE 3B – Power at Filter Output and Amplifier dc Current Versus Power Input for Vdc = 13.6 V.

*Add approximately 0.35 dB to power output values to determine power being delivered by the MRF226 output transistor.

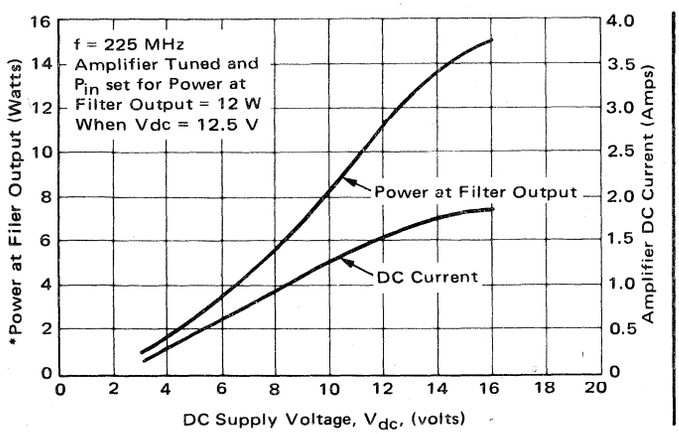


FIGURE 3C – Power at Filter Output and Amplifier dc Current as a Function of Variable dc Supply Voltage

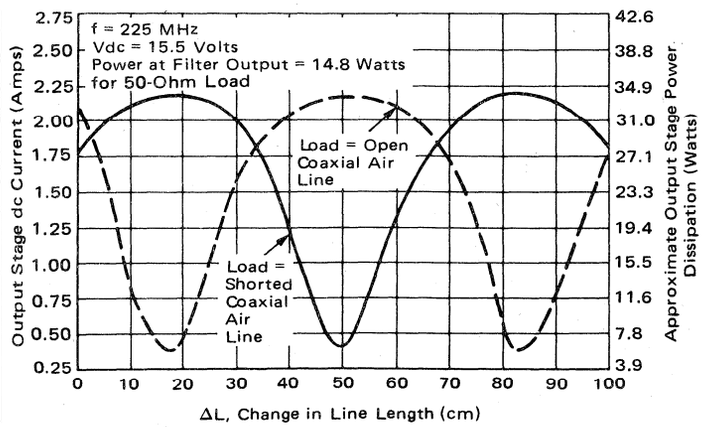


FIGURE 3D – Amplifier Output Stage dc Current and Power Dissipation for Open and Short Circuit Load Conditions at High Line Voltage

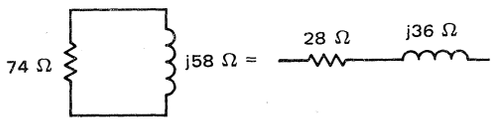
resistance value much lower than that required for normal 50 Ω load operation to keep the device junction temperature below its maximum specified value of 200°C. In practice, this worst case dissipation will rarely happen. Even if an open or short circuit malfunction should occur, it would have to be located at specific distances from the amplifier output and also a high dc line voltage must exist concurrently with the peak dc current. Any RF loss in the cable between the amplifier output and the short or open location will also reduce the severity of the situation.

If desired, protection circuitry can be designed into the amplifier which will automatically provide a reduction in RF drive power, supply voltage, or dc supply current during high VSWR load conditions and thus limit the worst case device dissipation to more acceptable levels.

RF DESIGN

A design procedure using the Smith chart, as detailed in Reference 2, can be used to synthesize the amplifier impedance matching networks. Since the reference provides an example network for matching to 50 Ω (similar to the amplifier input and output networks), it will suffice to only extend the procedure to include the MRF225 and MRF226 interstage network. Figure 4 shows the elements to be considered.

L2 provides the necessary base return for class C operation of the output stage. The combination wire coil and ferrite bead is optimized for circuit stability. The equivalent circuit values for the combination at 225 MHz are:



C5 is used to resonate out the inductive impedance of L2 and the MRF226 input. The resulting capacitive impedance provides a lower impedance ground return at the transistor base for harmonic currents.

In addition to providing the collector dc feed, L1 provides collector loading at frequencies below approximately 40 MHz to improve stability in this region where device gains have increased substantially. R2 serves to lower the otherwise high Q of L1.

The network of Figure 4A is reduced to that of Figure 4B by using the series/parallel conversion equations of Appendix A to combine the 225 MHz values of L1, L2 and C5 with the respective MRF225 and MRF226 impedance data. R2 has a negligible loading effect and can be ignored. The remaining impedance transformation network consisting of Z2, Z3, C3 and C4 is configured to provide dc isolation and to permit the ground return of C4 to be located near the output transistor emitter. The two transmission line section design permits an efficient transfer of power between the significantly different source and load impedances. Since extreme wideband performance is not a requirement of the amplifier, the network transmission line length and characteristic impedance can be chosen to facilitate circuit layout and to optimize performance at approximately 225 MHz. Line widths (62 mils) which result in characteristic impedances of 62.7 Ω have been used. Design values required for use with Reference 2 are summarized in Table III. They have been determined with the aid of the equations in Appendix B.

The Smith chart network solution using Table III values, and normalized for Z_0=62.7 Ω, appears in Figure 5. A portion of the constant-Q circles (dashed) have also been plotted.

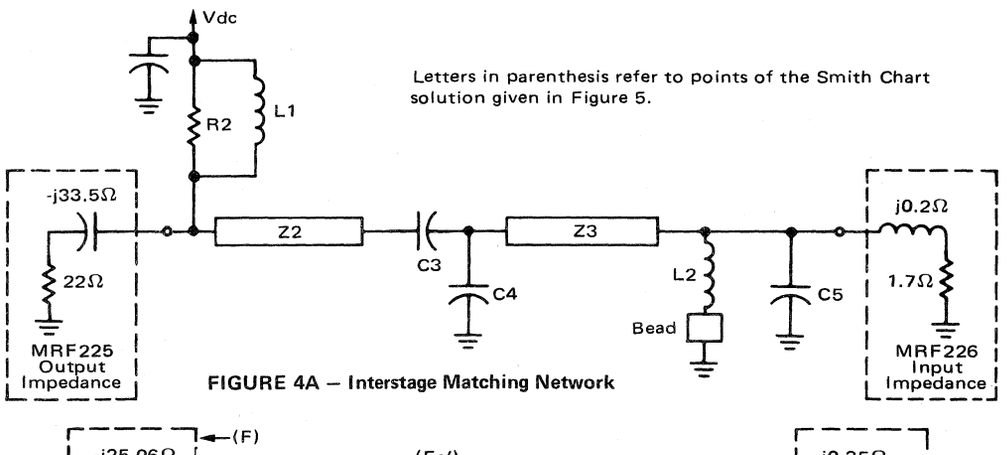


FIGURE 4A – Interstage Matching Network

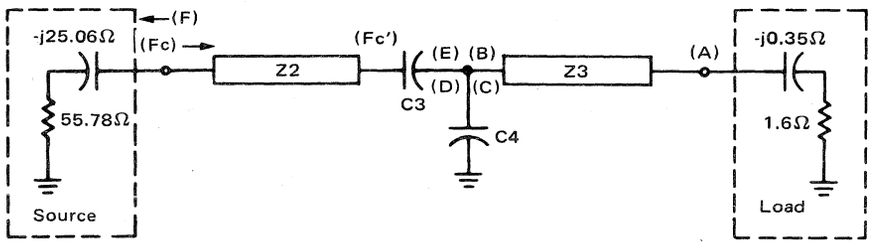


FIGURE 4B – Simplified Interstage Matching Network

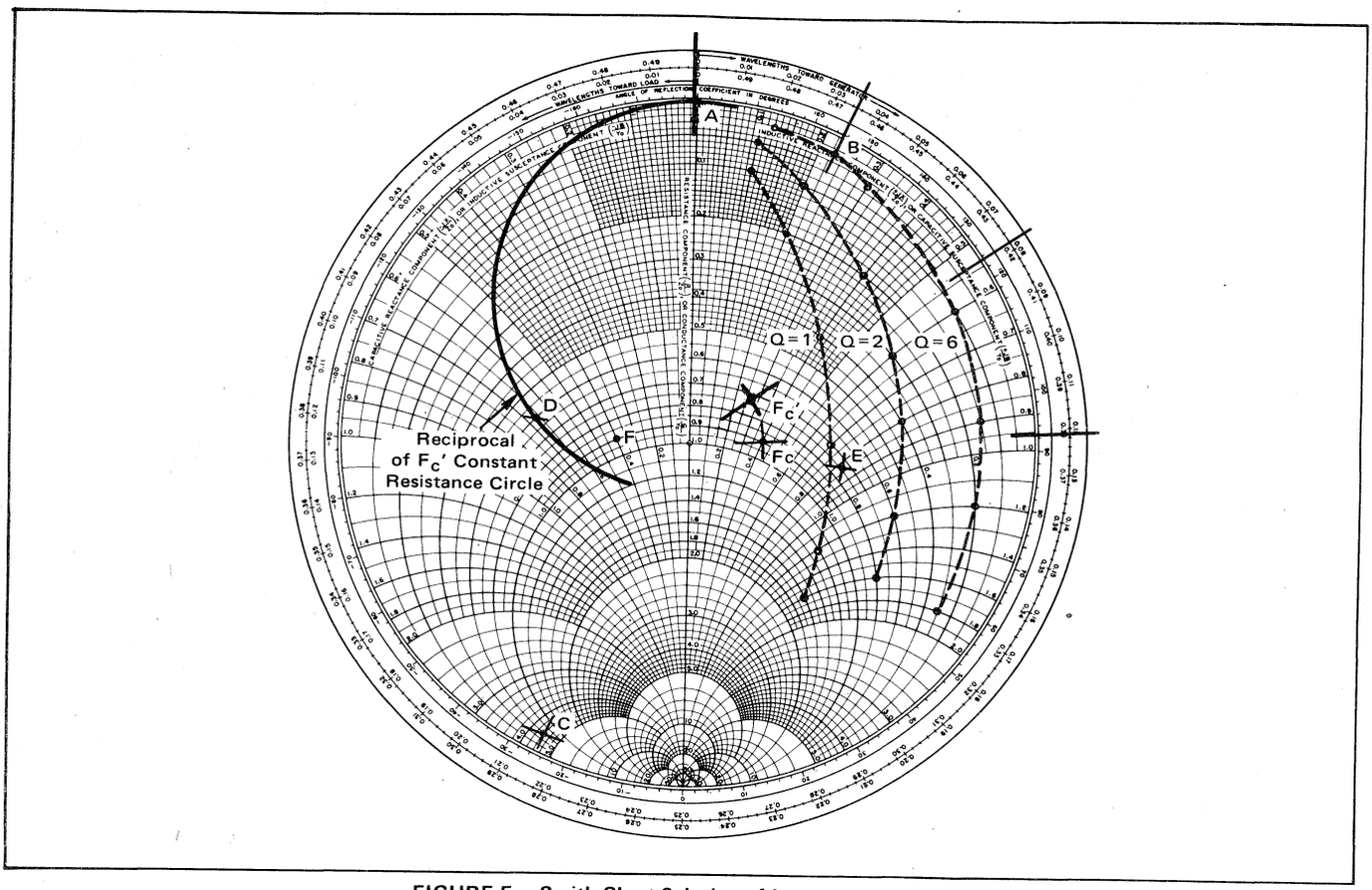


FIGURE 5 – Smith Chart Solution of Interstage Network

The normalized source impedance of Figure 4B is plotted at point (F); however, the matching network must present a conjugate match to the source for maximum power transfer, point (Fc). The normalized load impedance at (A) must therefore be transformed to (Fc). The network design can be summarized as follows:

(A) is rotated 0.036 λ toward the source to (B) by Z3. Similarly, (Fc) is rotated 0.043 λ toward the load to (Fc') by Z2. Converting (B) to an equivalent admittance results in point (C) located on the constant conductance circle of 0.60. Enough parallel susceptance must be provided by C4 to move (C) along its constant conductance circle towards the source until the reciprocal of the constant resistance circle of Fc' is intercepted. This occurs at (D). The amount of parallel susceptance required to move from (C) to (D) is:

$$\omega C_{CD}=(\omega C_C-\omega C_D)\,Y_0 = (4.4\text{-}0.67)\,\frac{1}{62.7}=59.5 \text{ mmho}$$

This results in a value for C4 of:

$$C4 = \frac{59.5 \times 10^{-3}}{2\pi \times 225 \times 10^6} = 42.1 \text{ pF.}$$

As indicated in Table II, this is well within the range of the Arco #403 trimmer when operating at 225 MHz .

Point (D) is transposed into an impedance (E) in order to determine the series reactance necessary to reach the desired impedance at (Fc'). Although (E) has the correct real part (0.74), it falls on the 0.84 reactance line while (Fc') lies on the 0.28 reactance line. The series reactance (provided by C3) to be added is, therefore:

$$(0.84\text{-}0.28)Z_0 = 0.56 \times 62.7 = 35.1\ \Omega$$

resulting in $C3 = \dfrac{1}{2\pi \times 225 \times 10^6 \times 35.1} = 20.1$ pF.

TABLE III – SUMMARY OF VALUES FOR USE IN INTERSTAGE NETWORK DESIGN

ϵ_r	=	PCB Dielectric Constant = 5
h	=	PCB Dielectric Thickness = 59.2 mils
t	=	PCB Copper Thickness = 1.4 mils
W	=	Width of Microstrip Line = 62 mils
Weff	=	Effective line width = 64.4 mils
Z_0	=	Line characteristic impedance = 62.7 Ω
λ_{TEM}	=	TEM mode wavelength @ 225 MHz = 59.5 cm
K	=	TEM mode correction factor = 1.19
λ'	=	Effective wavelength @ 225 MHz = 70.8 cm
λ2	=	Electrical length of Z2 = 0.043 λ
λ3	=	Electrical length of Z3 = 0.036 λ

Figure 4B Load Impedance of 1.6-j0.35 Ω is normalized to 0.026-j0.006 Ω.

Figure 4B Source Impedance of 55.78-j25.06 Ω is normalized to 0.89-j0.40 Ω.

A capacitor having a nominal low-frequency value of 15 pF is used for C3 since, as noted in Table II, it will exhibit an effective capacitance of approximately the calculated value at 225 MHz.

The Q of each point of the network plot can be determined from the constant-Q curves. The loaded Q for the total network will approximate that of the highest Q point and, in this case, will be approximately 6, as dictated by (B).

The low pass filter (C7, C8, C9, L4 and L5) represents a Tchebycheff network designed for 50 Ω source and load impedances, a 0.1 dB ripple, and a corner frequency of 250 MHz. Calculated values of 14.6 pF for C7 and C9, 25.1 pF for C8 and 43.6 nH for L4 and L5 are obtained (Reference 3). As indicated by Table II, capacitors having nominal low frequency values of 12 and 20 pF should be used.

THERMAL DESIGN

A good thermal analysis and the implementation of good thermal construction techniques are very important in RF power amplifier fabrication. A smooth heat sink surface and the stud torque specified by the transistor data sheet should be used when mounting stud-type transistor packages. Thermal joint compound should also be used between the transistor case and heat sink interface, (see Reference 4).

Heat sink thermal resistance ($R_{\theta SA}$) requirements for the amplifier transistors can be calculated using the dc current values from the test data in Figure 2, the RF power levels in Figure 1 and thermal data from Table IV in the following Equations.

$$P_D = P_{in(rf)} + P_{in(dc)} - P_{out(rf)} \quad (1)$$

$$R_{\theta JS} = R_{\theta JC} + R_{\theta CS} \quad (2)$$

$$R_{\theta SA} = \frac{T_J - T_A}{P_D} - R_{\theta JS} \quad (3)$$

TABLE IV – THERMAL DATA

DEVICE	$R_{\theta JC}$ °C/W	$R_{\theta CS}$ °C/W	$T_{J(max)}$ °C
MRF225	50	1	200
MRF226	3.89	*0.3	200

$R_{\theta JC}$ = Junction-to-Case Thermal Resistance

$R_{\theta CS}$ = Case-to-Heat Sink Thermal Resistance. Values Given Apply when Thermal Compound is Used

$T_J(max)$ = Maximum Permitted Junction Temperature

*Assumes Mounting Stud Nut Torqued at 6.5 in./lb.

For 12.5 V, 50 Ω load operation with an ambient temperature (T_A) of 60°C, calculations for the MRF226 output device yield:

$$P_D = 1.3 + 18.75 - 13.0 = 7.05 \text{ W} \quad (4)$$

$$R_{\theta JS} = 3.89 + 0.3 = 4.2°C/W \quad (5)$$

$$R_{\theta SA} = \frac{150\text{-}60}{7.05} - 4.2 = 8.5°C/W \quad (6)$$

A device junction temperature (T_J) of 150°C has been used in the $R_{\theta SA}$ calculation (maximum rated junction temperature is 200°C). Continuous operation under mismatched load conditions can result in a radical increase in device dissipation (P_D), thus causing a much lower heat sink thermal resistance requirement (see Performance Section).

Calculations for the MRF225 input stage transistor for similar conditions give an $R_{\theta SA}$ value of 57°C/W.

The $R_{\theta SA}$ values have been computed for continuous amplifier operation. The requirements will be reduced for less than 100 per cent duty cycle conditions. The input and output stage heat sinks pictured in the title illustration exhibit respective thermal resistance values of approximately 60 and 3.0°C/W in free air.

CONSTRUCTION

The amplifier has been constructed on a 2.10" X 4.05" X 0.062" double-sided printed circuit board of G10 dielectric material (ϵ_r=5). All component locations are accurately determined by the full scale layouts given in Figure 6.

Eyelet construction has been employed to eliminate the need for cumbersome wrap-around-grounds and/or expensive plated through holes. USM Corporation S-6064 and S-6084 size eyelets have been used to accommodate the different component lead diameters. Some of the eyelets (including three near the MRF226 emitter connections) are not used to accept component leads but are used to provide additional tie points between the top and bottom ground planes. If desired, plated-through holes can be used in place of the eyelets.

Most of the components can be inserted into the board and then secured using wave-soldering techniques for high volume economy. All fixed-value capacitors must be placed flush against the board to minimize lead length and to assure close correlation with the required capacitance values. The input stage T0-39 package should be placed near the printed circuit board surface to minimize emitter lead length. A transistor pad can be used to provide proper electrical isolation between the package and board circuit pattern. The MRF226 SOE case should be properly secured to its heat sink prior to soldering the device leads into the circuit, as discussed in Reference 4.

REFERENCES

1. "Systemizing RF Power Amplifier Design," by Roy Hejhall, Application Note AN-282A.
2. "Microstrip Design Techniques for UHF Amplifiers," by Glenn Young, Application Note AN-548A.
3. "A Handbook on Electrical Filters," by White Electromagnetics, Inc.
4. "Mounting Stripline-Opposed-Emitter (SOE) Transistors," by Lou Danley, Application Note AN-555.

APPENDIX A
SERIES AND PARALLEL EQUIVALENTS

To convert a parallel resistance and reactance combination to series:

$$R_S = \frac{R_P}{1 + \left(\frac{R_P}{X_P}\right)^2}, \quad X_S = \frac{X_P}{1 + \left(\frac{X_P}{R_P}\right)^2} \qquad (1)$$

To convert a series resistance and reactance combination to parallel:

$$R_P = R_S + \frac{(X_S)^2}{R_S}, \quad X_P = X_S + \frac{(R_S)^2}{X_S} \qquad (2)$$

APPENDIX B
TRANSMISSION LINE RELATIONS

$$Z_o = \frac{377h}{\sqrt{\epsilon_r} \times W_{eff}\left[1 + 1.735\,\epsilon_r^{-.0724}\left(\frac{W_{eff}}{h}\right)^{-.836}\right]} \qquad (1)$$

$$W_{eff} = W + \frac{t}{\pi}\left(\ln\frac{2h}{t} + 1\right) \qquad (2)$$

$$\lambda_o = \frac{c}{freq} = \frac{3 \times 10^8}{2.25 \times 10^8} = 1.33 \text{ meters} \qquad (3)$$

where c = propagation constant, free space

$$\lambda_{TEM} = \lambda_o/(\epsilon_r)^{1/2} \qquad (4)$$

$$K = \left[\frac{\epsilon_r}{1 + 0.63\,(\epsilon_r - 1)\left(\frac{W_{eff}}{h}\right)^{.1225}}\right]^{1/2} \qquad (5)$$

$$\lambda' = (\lambda_{TEM})(K) \qquad (6)$$

where λ' = effective wavelength

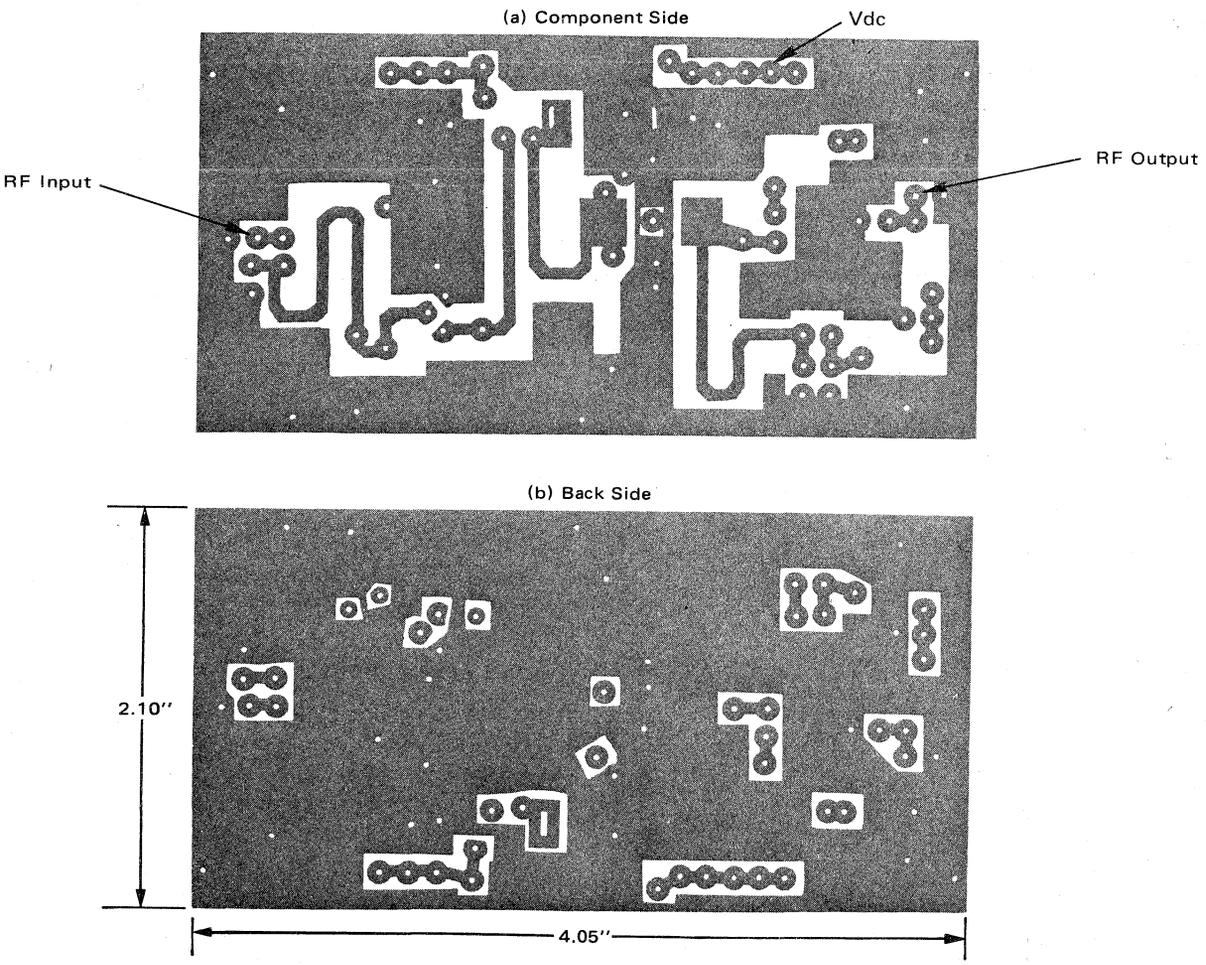


FIGURE 6 — Printed Circuit Board Artwork for 225 MHz Amplifier/Low Pass Filter

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Printed in Switzerland 11M